## **GF28: subLVDS**



#### Libraries

Name	Process	Form Factor
RGO_GF28_18V18_SLP_UC_SUBLVDS	SLP	Staggered
RGO_GF28_18V18_HPP_UC_SUBLVDS	HPP	Staggered

## **Summary**

The subLVDS library provides a subLVDS driver, receiver, and temperature stable voltage reference capable of supporting 16 drivers operating at data rates up to 1 Gbps. The pad set includes a full complement of power, spacer, and adapter cells to assemble a complete pad ring by abutment. An included rail splitter allows isolated subLVDS domains to be placed in the same pad ring with other power domains while maintaining continuous VDD/VSS in the pad ring for robust ESD protection.

- 250 MHz LVDS Driver
- 450 MHz LVDS Receiver
- subLVDS Voltage Reference

#### subLVDS Specification Compliant:

• SMIA 1.0 PART 2: CCP2 Specification

#### **ESD Protection:**

- JEDEC compliant
  - o 2KV ESD Human Body Model (HBM)
  - o 200V ESD Machine Model (MM)
  - 500V ESD Charge Device Model (CDM)

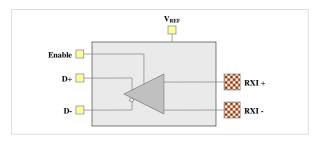
### **Absolute maximum ratings**

Symbol	Description	Value	Units
$V_{VDD}$	Core supply voltage range	-0.5 to 1.2	V
$V_{\text{DVDD}}$	I/O supply voltage range	-0.5 to 2.95	V
$V_{PAD}$	Voltage range at PAD	$-0.5$ to $(V_{DVDD} + 0.5)$	V
TJ	Junction operating temperature range	-55 to 150	°C

## **Recommended operating conditions**

Symbo	ol Description	Min	Nom	Max	Units
V <sub>VDD</sub> Core supply voltage		SLP	0.90	1.0	1.10
	SLP	0.99	1.1	1.155	
	Core supply voltage	HPP	0.765	0.85	0.935
		пРР	0.81	0.9	0.945
$V_{DVDD}$	I/O supply voltage	1.62	1.80	1.98	V
V <sub>VREF</sub>	Reference voltage		0.9		V
TJ	Junction temperature	-40	25	125	°C
V <sub>PAD</sub>	Voltage at PAD	-0.3V		V <sub>DVDD</sub> +0.3V	V

## LDP\_IN\_800\_18V\_DN: 1GHz subLVDS Input



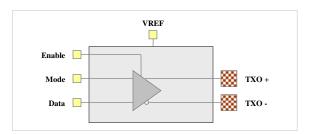
#### subLVDS Receiver Features:

- Input receive sensitivity of 50mV peak differential (without hysteresis)
- Common mode range from 0.4V to 1.4V (limited by Power Supply)
- Duty Cycle Distortion (DCD) less than 50ps
- Power consumption: 1.7 mW typical / 4.7 mW maximum

#### **AC Characteristics**

Parameter	Тур	Max	Units	Conditions
Propagation Delay	0.5	8.0	ns	The slew rate for propagation delays, duty cycle distortion and maximum operating frequency is 1V/ns
Maximum Operating Frequency	1.0		GHz	All noise, jitter, and tdcd measured at 1GHz
Maximum Data Rate	2.0		Gb/s	

## LSP\_OU\_800\_18V\_T: 1GHz subLVDS Output



## subLVDS Driver Features:

- Operates up to 1.0GHz (2.0 Gbps) with external 1pF load
- Common mode output range: 0.90V +/-50mV
- Differential Skew between TXO\_P and TXO\_N: 50ps
- High and low current drive modes to support  $50\Omega$  and  $100\Omega$  differential terminations
- Power consumption at 1GHz: 8.5 mW typical / 15.2 mW maximum

#### **AC Characteristics**

Symb	ol Description	Condition	Min	Тур	Max	Units
t <sub>PHL</sub>	Differential high to low propagation delay	$R_L = 100 \Omega$ $C_L = 1 pF$		480	710	ps
t <sub>PLH</sub>	Differential low to high propagation delay	$R_L = 100 \Omega$ $C_L = 1 pF$		480	710	ps
trise	VoD differential rise time	20% to 80%	120		250	ps
t <sub>fall</sub>	V <sub>OD</sub> differential fall time	20% to 80%	120		250	ps

# **GF28: subLVDS Pad Set**



### **Cell summary**

Name	Description
LDP_IN_800_18V_DN	1GHz SubLVDS input cell
LSP_OU_800_18V_T	1GHz SubLVDS output cell
LDP_RE_009_18V	V <sub>REF</sub> pad
PVP_VD_RCD_10V	Core power pad with VREF
PVP_VS_RCD_10V	Power pad for VSS with VREF bus
PVP_VD_PDO_18V	Driver power pad with POC control
PVP_VD_RDO_18V	Driver power pad
PVP_VS_RDO_18V	I/O ground supply with VREF bus
SVP_SP_001_18V	0.1 µm spacer
SVP_SP_001_18V	1 µm spacer
SVP_SP_005_18V	5 μm spacer
SVP_SP_010_18V	10 µm spacer
SPP_RS_005_18V	DVDD, DVSS, POC, BIAS and VREF rail splitter
SPC_SPC_AD_UN	Core limited library adapter pad

## **Physical sizes**

Pad name	Width	Height <sup>[*]</sup>	Units
LDP_RE_009_18V	40	139	μm
LDP_IN_800_18V_DN	40	117	μm
LSP_OU_800_18V_T	50	129	μm
PVP_VD_RCD_12V	20	117	μm
PVP_VS_RCD_12V	20	117	μm
PVP_VD_PDO_18V	20	117	μm
PVP_VD_RDO_18V	20	117	μm
PVP_VS_RDO_18V	20	117	μm
SVP_SP_000_18V	0.1	117	μm
SVP_SP_001_18V	1	117	μm
SVP_SP_005_18V	5	117	μm
SVP_SP_010_18V	10	117	μm
SPP_RS_005_18V	5	117	μm
SPP_SPC_AD_UN	20	117	μm

<sup>[\*]</sup> Includes CUP bond opening.

### **Characterization Corners**

Nom VDD	Model	VDD	DVDD=1.8V	Temperature
	FF	+5%	+10%	-40°C
	FF	+5%	+10%	125°C
1.1 (SLP)	TT	nominal	nominal	25°C
(OLI)	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
	FF	+10%	+10%	-40°C
4.0	FF	+10%	+10%	125°C
1.0 (SLP)	TT	nominal	nominal	25°C
(OLI)	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
	FF	+5%	+10%	-40°C
0.0	FF	+5%	+10%	125°C
0.9 (HPP)	TT	nominal	nominal	25°C
(1111)	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
0.85 (HPP)	TT	nominal	nominal	25°C
(1111)	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

#### © 2006-2019 Aragio Solutions. All rights reserved.

Information in this document is subject to change without notice. Aragio Solutions may have patents, patent applications, trademarks, copyrights or other intellectual property rights covering subject matter in this document. Except as expressly provided in any written license agreement from Aragio, the furnishing of this document does not give you any license to the patents, trademarks, copyrights, or other intellectual property.

#### Published by:

Aragio Solutions
2201 K Avenue
Section B Suite 200
Plano, TX 75074-5918
Phone: (972) 516-0999
Fax: (972) 516-0998
Web: http://www.aragio.com/

While every precaution has been taken in the preparation of this book, the publisher assumes no responsibility for errors or omissions, or for damages resulting from the use of the information contained herein. This document may be reproduced and distributed in whole, in any medium, physical or electronic, under the terms of a license or nondisclosure agreement with Aragio.

Printed in the United States of America

Jun-2019